Remarks/Arguments

Claims 1-26 are pending in the application. Claims 1-26 are rejected.

Claim Rejections 35 USC § 102

Claims 1, 2, 5, 6, 7, 9-12, 15-19, 22-24 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Kitsukawa et al., US Patent 5,844,853.

Claims 3, 4, 8, 13, 14, 20, 21 and 25 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kitsukawa et al., US Patent 5,844,853.

It was previously argued that if 8a and 8b were to operate together, it was disclosed that they receive their signals from a same I/O port of the IC and us such must be within a same IC to work together (as disclosed). Thus, the reference could not anticipate Applicant's claims.

Though a detailed analysis of the reference cited did not appear necessary since it clearly fails to disclose the circuits 8a and 8b operating on separate dies one in conjunction with another, the objection has been maintained necessitating a more complete explanation of the reference.

In particular Kitsukawa relates to master slice technique ASIC manufacturing of DRAM. Understanding the term "master slice" is required to put perspective on the reference.

In prior art ASIC design, it was common to design a single use/function circuit. Thus, ASIC designs were highly customized allowing for specific application use. To provide two versions or configurations of a design required two custom designed ASICs. Thus, providing two configurations would require twice the non-recoverable engineering expense and so forth. Hence, a typical ASIC had only one configuration.

Another approach to providing two configurations for a same design is to provide both configurations in a same ASIC. For example, a same ASIC supports 2 different frequencies of operation selectable by, for example, a voltage on an external pin thereof.

Unfortunately, there are many applications wherein one use or configuration is mutually exclusive of another and, as such, two different ASICs are still necessary to achieve both configurations. As Kitsukawa explains, for the DRAM application disclosed a 3.3V and a 2.5V configuration are mutually exclusive due to requirements of each. For example, dielectric leakage characteristics and memory cell stability issues are affected by the operating voltage and, therefore, render two operating voltage configurations for a same ASIC non-trivial.

Master Slice is a term used to refer to a first product of the ASIC manufacturing process – the wafer. When applying Master Slice techniques to ASIC design, one designs a master slice that serves functionally for both configurations. Typically, the master slice comprises a wafer having the active components within the semiconductor – transistors, diodes, etc. In a subsequent processing step, a circuit with a specified function is accomplished by adding a final surface layer or layers of metal interconnects to the master slice late in the manufacturing process, joining the active elements allows the designed function of a chip to be implemented. As is well known in the art, different metal interconnects are useful in implementing different resulting ASICs relying on a same master slice. Thus, by wiring the active components differently, a different chip results having different characteristics.

In U.S. Patent 5,844,853, Kitsukawa discloses a DRAM circuit that is customizable through master-slice techniques (during manufacture) to result in a 2.5V or a 3.3V version (hence the use of the term version in the specification). Once manufactured, the DRAM is fixed as either a 2.5 volt DRAM or a 3.3 volt DRAM. Thus, the two circuits never operate cooperatively nor are either of them manufactured having more than one die.

Essentially, a wafer is formed having the active components therein and Kitsukawa discloses how to couple the active components to form a 2.5V and how to couple the active components differently to form a 3.3V DRAM with the same master slice. According to Kitsukawa the configurations avoid at least some of the prior art limitations of implementing an identical 3.3V and 2.5V version.

There is no teaching in Kitsukawa of anything that would read on the invention as claimed

in claim 1. I note some specific features not disclosed by Kitsukawa (highlighting my own), though these do not represent an exhaustive list of distinctions.

1. An electronic apparatus comprising:

a **first integrated circuit semiconductor die** comprising:

a first signal conditioning circuit integrated within the first integrated circuit die for performing a first signal conditioning function on a signal propagating along a first signal path;

a first ancillary circuit integrated within the first integrated circuit die and electrically coupled to the first signal conditioning circuit for other than performing the first signal conditioning function and for use by the first signal conditioning circuit during operation thereof;

a second integrated circuit semiconductor die comprising a second signal conditioning circuit integrated within the second integrated circuit die for performing a second signal conditioning function on a signal propagating along a second signal path that is different than the first signal path;

a second ancillary circuit integrated **within the first integrated circuit semiconductor die** and electrically coupled to the second signal conditioning circuit for other than performing the second signal conditioning function and for use by the second signal conditioning circuit during operation thereof;

a **substrate for supporting the first and second integrated circuit semiconductor dies** and for providing electrical connection to and from the first and second integrated circuit semiconductor dies.

Thus, a careful review of the teachings of Kitsukawa shows why there is no specific mention of 8a and 8b functioning cooperatively. It is because this is not taught. In fact, it is effectively precluded since you only have version 8a OR version 8b. Since the Examiner sites 8a as one die and 8b as the second die, the objection makes little technical sense in view of the purpose and teachings of Kitsukawa. Further, to anticipate a reference requires that the reference teach each and every element of the claimed invention, which is clearly not the case. As such, Applicant traverses the present objections.

The application is now believed to be in proper condition for allowance. Applicant looks forward to receiving favorable reconsideration of the present application.

Please charge any additional fees required or credit any overpayment to Deposit Account No. 20-1430.

Respectfully submitted,

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